

Subject Title : LOGIC DESIGN LAB		
Subject Code : CSL37	No. of Credits : 1.5=0 : 0 : 1.5 (L-T-P)	No. of lecture hours/week : 3
Exam Duration : 3 Hours	CIE + SEE = 50 + 50 =100	

Course Objectives:

This course will help students to achieve the ability to:

1. Design and implement different logic design circuits using components like logic gates, multiplexer, decoder, flip-flops IC's.
2. Use of computer-aided design tools for simulation.

Expt No.	Experiment List
1	a) Given a 4-variable logic expression, simplify it using K-Map and realize using universal gates. b) Simulate the simplified logic expression using VHDL and verify its working.
2	a) Design and implement a combinational circuit (Adder, Subtractor, Magnitude Comparator) using logic gates. b) Simulate the above combinational circuit using VHDL and verify its working.
3	a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC. b) Simulate 4:1 multiplexer using VHDL and verify its working.
4	a) Realize given Boolean expression using 3:8 Active low output decoder. b) Simulate 2:4 Decoder using VHDL and verify its working.
5	a) Realize Master Slave JK Flip Flop using NAND gates. (OR) b) Simulate D Flip Flop using VHDL and verify its working.
6	a) Design and implement a ring counter using 4-bit shift register and demonstrate its working. b) Simulate switched tail counter using VHDL and verify its working.
7	a) Design and implement an asynchronous counter using decade counter IC to count up from 0 to n ($n \leq 9$) and demonstrate its working.
8	a) Design and implement a mod-n ($n < 8$) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working (OR) b) Simulate mod-8 counter using VHDL and verify its working.

Course Outcomes:

Students are expected to do the following.

1. Understand, Analyze, Design, and implement different combinational and sequential logic circuits.
2. Simulation and analysis of logic circuits using VHDL.

Cos	Mapping with POs
CO1	PO1, PO2, PO3, PO4, PO5, PO12
CO2	PO1, PO2, PO3, PO4, PO5, PO12