Subject Title : **LOGIC DESIGN**		
Subject Code : CS31	No. of Credits : ::4=4 : 0 : 0 (L-T-P)	No of Lecture Hour/week : 4
Exam Duration : 3 Hours	CIE +Assignment + SEE = 45 + 5 + 50 =100	Total No. of Contact Hours :52

Course Objectives:

1 Understand the basic digital principles and working of various logic gates, and different techniques for simplification of Boolean function.
2. Understand combinational logic circuits, design and applications.
3. Understand Flip Flops, synchronous and Asynchronous sequential circuits.

Unit No.	Syllabus content	No. of hours
1	Digital Principles, Digital Logic The Basic Gates: NOT, OR, AND, Universal Logic Gates: NOR, NAND, implementation of circuits using NAND and NOR, Combinational logic, Truth table representation, canonical forms, Karnaugh maps, minimization of complete Boolean functions and incomplete Boolean functions using K-Map.	10
2	Digital Principles, Digital Logic Contd.,: Quine-McCluskey method, determination of prime implicants, prime implicates, finding minimal sum and minimal product using QM-method. Combinational Logic: Adder, subtractor, code convertors, magnitude comparator.	10
3	Data processing circuits: Multiplexers, Demultiplexers, Decoder, Encoders, Programmable logic devices, Programmable Array Logic, Programmable Logic Arrays.	10
4	Latches and Flip Flops: Introduction, Set Reset Latch, Gated Latch, Clocked D FLIP-FLOP, Edge-triggered D FLIP-FLOP, S-R FLIP FLOP, T FLIP FLOP,JK FLIP-FLOP, JK Master-slave FLIP-FLOP, Flip- Flop characteristics equations and excitation table.	11
5	Registers and counters: Introduction, registers, shift registers, ripple counters, synchronous counters, Fundamentals of sequential design: general models for sequential circuits, Design of Synchronous Sequential Circuit, Model Selection, State Transition Diagram, State Synthesis Table, Design Equations and Circuit Diagram.	11

Note 1: Unit 1, 2, 3 will have one question each.
Note 2: Unit 4 and Unit 5 will have internal choice.
Note 3: Three assignments are evaluated for 5 marks:

Assignment - 1 from units 1 and 2.
Assignment - 2 from units 3 and 4.
Assignment - 3 from unit 5.

Course Outcomes:

This course uses assigned readings, lectures and homework to enable the students to:

1. Understand the working of various logic gates, K-map, Quine-McCluskey method and flip flops and demonstrate the minimization of combinational functions using varioustechniques like K-map, Quine-McCluskey method.
2. Analyze and Design different combinational circuits.
3. Analyze and design different sequential circuits using flip flops, synchronous sequential acircuits using Mealy and Moore model.

Cos	Mapping with POs
CO1	PO1,PO2,PO3,PO4,PO5,PO12
CO2	PO1,PO2,PO3,PO4,PO5,PO12
CO3	PO1,PO2,PO3,PO4,PO5,PO12

Text Book:

1. Fundamentals of logic design, Charles H.Roth, Jr.Cengage Learning, 5th edition, 2012. (Listed topic only from Units -4, 5, 6, 9, 11, 12, 13)
   ISBN: 978-1-133-62847-5
2. M Morris Mano: Digital Logic and Computer Design, 10th Edition, Pearson, 2008.
   ISBN: 978-8-120-30417-8 (Listed topic only from Units – 4, 6, 7)

Reference Books:

1. R D Sudhaker Samuel: Illustrative Approach to Logic Design, Sanguine-Pearson, 2010.
2. Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 7th Edition, Tata McGraw Hill, 2010.
3. Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss: Digital Systems Principles and Applications, 10th Edition, Pearson Education, 2007.